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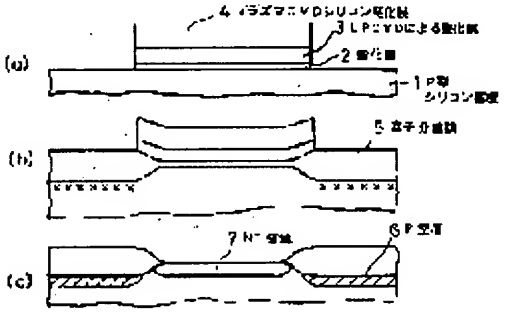
(54) MANUFACTURE OF ELEMENT ISOLATION REGION OF SEMICONDUCTOR

(57)Abstract:

PURPOSE: To prevent a channel stopper layer under an element isolation film of a semiconductor device from diffusing into an element forming region, and form a mask for ion implantation to form the channel stopper layer in a self alignment manner.

CONSTITUTION: When the element isolation region of a semiconductor device is formed, a low stress silicon nitride film 4 is thickly deposited by a plasma CVD method, on a silicon nitride film 3 deposited by an LPCVD method, and an element isolation film 5 is formed by patterning and thermally oxidizing the silicon nitride film. Then channel stopper ions are implanted through the element isolation film 5 by using the thick silicon nitride film as a mask.



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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of the component isolation region in the production process of a semiconductor device.
[0002]
[Description of the Prior Art] The manufacture approach of the conventional component isolation region is explained using drawing 3 .
[0003] LOCOS for which drawing 3 is usually used -- the manufacture approach of the component demarcation membrane by law is shown. According to drawing, it explains below. the P type silicon substrate 21 -- the thermal oxidation film 22 -- about 300A -- forming -- further -- LPCVD (Low Pressure Chemical Vaper Deposition) -- about 2000A of silicon nitrides 23 is deposited by law. It is boron (B+) as a channel stop ion implantation to the whole surface after carrying out patterning of the thermal oxidation film 22 and the silicon nitride 33. For example, 2x1013-/cm2 of 30KeV(s) It pours in on conditions. (With, above figure 3 a)
Next, 1000 degrees C and elevated-temperature heat treatment for about 120 minutes are carried out for a silicon substrate in an oxidizing atmosphere, and the about 5000A component demarcation membrane (the so-called field oxide) 24 is formed. (Drawing 3 b))
Next, the silicon nitride 23 is removed in a heat phosphoric acid, and the drug solution of a fluoric acid system removes the thermal oxidation film 12. Then, devices, such as a transistor and PN-junction diode, are formed on the exposed silicon front face. (Drawing 3 c))
N+P junction is shown as an example. This corresponds also to the source drain field of a transistor. As an approach, they are an arsenic (As+) or Lynn (P+) to the silicon substrate 21 whole surface. It is N+ by pouring in by the ion implantation on condition that 4x1015 ions/cm2 and 30KeV, and heat-treating about 20 minutes in 900 degrees C and nitrogen-gas-atmosphere mind after that. P type junction is formed.
[0004] However, especially with the approach described above, it is N+ at the A section of the edge (drawing 3 d) of the component demarcation membrane 24. The field and the P type field 26 where the concentration formed of the channel stop ion implantation is high contacted, and there was a trouble that a junction capacitance became large. This is because the P type field 26 where the concentration which is a channel stop layer inevitably is high is spread all over the outside of the component demarcation membrane 24, i.e., the silicon substrate for device formation, in order that hot heat treatment may enter after a channel stop ion implantation.
[0005] So, recently, it is 1990IEDM. The approach of performing a channel stop ion implantation after component demarcation membrane formation shown in P.647 to P.650 is proposed like. Hereafter, it explains using drawing 2 . About 300A of thermal oxidation film 12 is first formed in the P type silicon substrate 11, and also about 2000A of silicon nitrides 13 is deposited by the LPCVD method. After carrying out patterning of the thermal oxidation film 12 and the silicon nitride 13, without performing a channel stop ion implantation, 1000 degrees C and elevated-temperature heat treatment for about 120

minutes are performed for a silicon substrate in an oxidizing atmosphere, and the about 5000A component demarcation membrane 14 is formed. (Drawing 2 a))
Next, the silicon nitride 13 is removed in a heat phosphoric acid, and the drug solution of a fluoric acid system removes the thermal oxidation film 12. Then, a resist is applied to the whole surface, exposure development is carried out, and a resist pattern 15 is obtained. At this time, from the edge of a component demarcation membrane, the edge of a resist pattern 15 detaches only the predetermined distance L, and is formed. Subsequently, a resist pattern 15 is used as a mask and they are acceleration energy 220KeV and the 2x1013 ions/cm dose 2 about boron (B+) as a channel stop ion implantation. An ion implantation is performed on conditions. Then, impregnation ion attaches and escapes from the component demarcation membrane 14, and is poured into the bottom of a component demarcation membrane. (Drawing 2 b))
Next, a resist pattern 15 is removed. For example, if N+P junction is formed, they will be an arsenic (As+) or Lynn (P+). It pours in by the ion implantation on condition that 4x1015 ions/cm2 and 30KeV, and while N+P junction is formed by carrying out heat treatment for about 40 minutes in 900 degrees C and nitrogen-gas-atmosphere mind after that, channel stop ion is also activated and it becomes the channel stop P type layer 16. Since only distance L has separated from the edge of the component demarcation membrane 14 the edge of the resist pattern 15 which are carrying out the channel stop ion implantation and the mask of a channel stop ion implantation after performing elevated-temperature heat treatment at the time of forming the component demarcation membrane 14 so that clearly from drawing 2 c, it is N+. A field 17 and the P type layer 16 cannot contact, and can also stop a junction capacitance low.
[0006]
[Problem(s) to be Solved by the Invention] However, by the approach mentioned above, since the location which performs a channel stop ion implantation using the phot lithography method was limited, there was a trouble of being easy to produce a doubling gap etc. It is said N+ when a doubling gap becomes beyond the distance L. A field 17 and said P type layer 16 will contact, and a junction capacitance will become large.
[0007] Moreover, what it has troubles, such as a cost rise and lowering of the yield, and can satisfy it technically since ** resist spreading ** photo mask doubling ** exposure ** development ** resist clearance 5 process of a routing counter increases was not obtained.
[0008]
[Means for Solving the Problem] this invention -- component isolation region formation of a semiconductor device -- hitting -- LPCVD -- a low stress silicon nitride is thickly deposited by the plasma-CVD method on the silicon nitride deposited by law, and patterning of the silicon nitride is carried out after that, and heat treatment hot in the inside of an oxidizing atmosphere is performed, a component demarcation membrane is formed selectively, and it is made to pour in channel stop ion through a component demarcation membrane by using a silicon nitride thick after that as a mask
[0009]
[Function] According to this invention, after performing hot heat treatment, since it was made to perform a channel stop ion implantation for a thick silicon nitride on a mask, a channel stop diffusion layer can be formed in self align. Therefore, the trouble of lowering of the doubling gap by the phot lithography method and the cost rise yield by the increment in a process is solvable.
[0010]
[Example] Drawing 1 is the process sectional view of the manufacture approach which shows the example of this invention. The P type silicon substrate 1 is first heat-treated by the oxidizing atmosphere, and the about 300A oxide film 2 is formed. Then, about 1500A of silicon nitrides 3 is deposited by the LPCVD method. About 8000A of low stress silicon nitrides 4 is succeedingly deposited by the plasma-CVD method. A low stress silicon nitride sets flow rate of a silane, ammonia, and nitrogen to 140/60/1500SCCM respectively, and is 6.5Torr(s) and raising RF power about a pressure 2.5 W/cm2 If film deposition is performed under conditions with a lowering temperature of about 400 degrees C, it will be stress 5x108 dyne/cm2. The silicon and the rich silicon nitride of extent

are obtained. Since it was made to deposit a low stress silicon nitride as mentioned above in this invention, even if it thickens thickness with 8000A, it can prevent that the crack and defect by film stress enter. Then, an oxide film 2 and the silicon nitrides 3 and 4 are made to save only on a component formation field by the usual FOTORISO method and the usual etching method. (Drawing 1 a))
Next, if 1000 degrees C of heat treatments for about 90 minutes are performed and a silicon substrate is oxidized in a wet oxidizing atmosphere, the about 5000A component demarcation membrane 5 will be selectively formed on a component isolation region.
[0011] Next, boron used as channel stop ion (B+) Acceleration energy 220KeV and 2x1013 ions/cm dose 2 On conditions, the ion implantation of the low stress silicon nitride 4 is carried out to a mask on the whole surface. At this time, it is boron (B+). Range distance becomes about 5000A and is boron (B+) selectively only under a component demarcation membrane. It is poured in. The field with a thick silicon nitride is boron (B+) in a silicon nitride. Since it stops, it is not poured in into a silicon substrate. Moreover, since it is hidden in part and is formed also in the bottom of the silicon nitride 3 (the so-called BAZU beak), the edge of the component demarcation membrane 5 is boron (B+). Predetermined distance gap ****** is carried out from the edge of the component demarcation membrane 5 at a component isolation region side. (drawing 1 b)) Next a heat phosphoric acid removes the thick silicon nitride 4 and the lower layer silicon nitride 3, and the solution of a fluoric acid system removes the about 300A oxide film 2. Then, the PN junction of a transistor etc. is formed on the exposed silicon substrate. the approach usual in drawing -- an N type impurity -- an ion implantation -- carrying out -- N+ -- the case where P junction is created is shown. (Drawing 1 c))
Although channel stop ion explained [the silicon substrate] using the example of P type with P type above, it cannot be overemphasized that those conductivity types may be N type.
[0012]
[Effect of the Invention] Since according to the manufacture approach of this invention the thick silicon nitride has lapped with the edge of a component demarcation membrane, uses that thick silicon nitride as a mask and was made to perform a channel stop ion implantation in self align as explained to the detail above, there are neither buildup of the junction capacitance by doubling gap of HOTORISO, nor the cost rise by the increment in a routing counter, yield lowering, etc.
[0013] Furthermore, since a channel stop layer can be formed in self align, it is usable also to high integration of a semiconductor device.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] The process which forms a comparatively thin oxide film in the component formation field on the 1 principal plane of a silicon substrate, The process which forms a comparatively thin silicon nitride by the reduced pressure chemical-vapor-deposition method (LPCVD) on said comparatively thin oxide film, and on said comparatively thin silicon nitride, by plasma chemistry vapor growth low -- with the process which forms a thick stress silicon nitride, and said comparatively thin silicon nitride low -- with the process which oxidizes a silicon substrate thermally by using a thick stress silicon nitride as an anti-oxidation mask, and forms a thick component demarcation membrane A thick stress silicon nitride is used as a mask.'said comparatively thin nitride and low -- The component isolation region formation approach of the semiconductor device characterized by giving the process which carries out the ion implantation of the impurity of the same conductivity type as said silicon substrate through said thick component demarcation membrane, and forms a channel stop field one by one.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The process sectional view showing the manufacture approach of this invention
[Drawing 2] The process sectional view showing the conventional manufacture approach (1)
[Drawing 3] The process sectional view showing the conventional manufacture approach (2)
[Description of Notations]
1, 11, 21 P type silicon substrate
2, 12, 22 Oxide film
3, 13, 23 Silicon nitride
4 Plasma-CVD Silicon Nitride
5, 14, 24 Isolation oxide film
6, 16, 26 Deep P type layer
7, 17, 25 N+ Field
15 Resist Pattern

[Translation done.]